METHOD FOR PACKAGING A SEMICONDUCTOR DEVICE

Field of the Invention

The present invention relates to a method for packaging a semiconductor device; and, more particularly, to a method for interconnecting a chip with a substrate in a semiconductor device by performing a flip-chip bonding by forming an Au bump on a bond pad of the chip, thereby enabling a miniaturization of the semiconductor device and a simplification of the packaging process.

Background of the Invention

Fig. 1 illustrates a sectional view of a BGA package fabricated in accordance with a packaging method of the prior art. As shown in Fig. 1, in accordance with the prior art, a chip 106 is attached to a substrate 100 through an adhesive 102. Thereafter, the chip 106 is interconnected with the substrate 100 through a gold wire 104. Then, the chip 106 and the gold wire 104 are encapsulated and sealed by using an epoxy molding compound 108. Solder balls 110 are then attached to the substrate 100. Subsequently, the substrate is sawed to singulate individual packages, by which a fabrication of the BGA package is completed.

In the BGA package as shown in Fig. 1, a flip-chip

bonding is performed by attaching solder balls to a bond pad of the substrate, which requires subsequent a flux printing process and a deflux process. Therefore, the fabrication process of the BGA package becomes complicated and it is hard to miniaturize the package.

Summary of the Invention

It is, therefore, an object of the present invention to provide a method for packaging a semiconductor device wherein a chip and a substrate is interconnected by performing a flip-chip bonding through an Au bump formed on a bond pad of the chip, thereby enabling a miniaturization of the device and a simplification of the packaging process.

In accordance with a preferred embodiment of the present invention, there is provided a method for packaging a semiconductor device, including the steps of: (a) forming an Au bump on a bond pad of a wafer; (b) dicing the wafer into a chip; (c) attaching the chip to a substrate to form a flip-chip bonding therebetween by using a thermo-pressure process; (d) encapsulating the flip-chip bonding by using a nonconductive epoxy; and (e) sawing the substrate to singulate individual packages.

Brief Description of the Drawings

The above and other object and features of the present invention will become apparent from the following description of preferred embodiments given in conjunction with the accompanying drawings, in which:

Fig. 1 describes a sectional view of a BGA package fabricated by using a method in accordance with the prior art;

Fig. 2 depicts a sectional view of a BGA package fabricated by using a method in accordance with a preferred embodiment of the present invention;

Fig. 3A illustrates an enlarged sectional view of an Au bump formed on a bond pad of the chip shown in Fig. 2; and

Fig. 3B provides an enlarged sectional view of a plating lead formed in the substrate shown in Fig. 2.

Detailed Description of the Preferred Embodiment

Fig. 2 illustrates a sectional view of a BGA package fabricated by using a method in accordance with a preferred embodiment of the present invention. In the following, the method of the present invention will be described in detail with reference to Fig. 2.

As shown in Fig. 2, an Au bump 200 is deposited on a

bond pad formed on a wafer. The wafer is then diced into a chip 202, which is attached to a substrate 204 by using a thermo-pressure process. An electrical connection of the chip 202 to an external device, i.e., a flip-chip bonding is completed through the thermo-pressure process.

As shown in Fig. 3A, the Au bump 200 formed on the chip 202 may be attached to the substrate 204 through an Ag layer 300 and a Cu layer 302.

Meanwhile, a plating lead B positioned on a lower part of the substrate 204 is connected to the Au bump 200 through a Cu pattern 306. As shown in Fig. 3B, the plating lead B is formed by plating an AgSn layer on the Cu pattern 306.

Thereafter, the flip-chip bonding is encapsulated by using a nonconductive epoxy and then the substrate 204 is sawed to singualte individual packages.

As described above, in accordance with present invention, a wire-bonding process and a molding process using an epoxy molding compound are not required. Further, a process of attaching solder balls to the substrate is not required, which eliminates subsequent flux printing and deflux processes. Accordingly, a packaging process of a semiconductor device becomes simplified and therefore the cost of the semiconductor device is decreased.

While the invention has been shown and described with respect to the preferred embodiments, it will be understood by those skilled in the art that various changes and

modifications may be made without departing from the spirit and scope of the invention as defined in the following claims.